AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

What is claimed is:

1. (Original) In a multi-threaded processor for at least first and second threads, a method of assigning thread priority comprising:

assigning priority to said first thread;

loading a preliminary value to a thread precedence counter; and

assigning priority to said second thread in response to expiration of said thread precedence counter.

2. (Original) The method of claim 1 wherein said preliminary value is based on a value stored in a first starting counter associated with said first thread.

3. (Original) The method of claim 2 further comprising:

determining if there is an indication of approaching instruction side starvation for said first thread; and

incrementing a value stored in said first starting counter in response to an indication of approaching instruction side starvation for said first thread.

4. (Currently Amended) The method of claim 3 wherein determining if there is an indication of approaching instruction side starvation for said first thread includes

determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

5. (Original) The method of claim 4 wherein when incrementing the value stored in the first starting counter, said value is incremented geometrically.

6. (Original) The method of claim 5 wherein said value is incremented geometrically by left-shifting a binary 1 bit into said value.

7. (Currently Amended) In a multi-threaded processor to handle processing of at least first and second threads, a method of assigning thread priority comprising:

assigning priority to said first thread; and

assigning priority to said second thread in response to one of a plurality of conditions being true, the conditions ~~including~~ consisting

if a thread precedence counter expires;

if processing of said first thread retires an instruction from said first thread; and

if there is not an indication of approaching instruction side starvation for said first thread.

8. (Currently Amended) The method of claim 7 wherein said indication of approaching instruction side starvation for said first thread includes each of a plurality of conditions being true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

9. (Original) A processor to handle processing of at least first and second threads in parallel, comprising:

control logic to assign priority to one of said at least first and second threads;

a thread precedence counter coupled to said control logic wherein priority is assigned to said second thread after said thread precedence counter expires.

10. (Original) The processor of claim 9 wherein a preliminary value for said thread precedence counter is based on a value stored in a first starting counter associated with said first thread.

11. (Original) The processor of claim 10 wherein said control logic is to determine if there is an indication of approaching instruction side starvation for said first thread and to increment a value stored in said first starting counter if there is an indication of approaching instruction side starvation for said first thread.

12. (Currently Amended) The processor of claim 11 wherein said control logic is to determine if there is an indication of approaching instruction side starvation for said first thread by determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

13. (Original) The processor of claim 12 wherein said control logic is to increment the value stored in the first starting counter geometrically.

14. (Original) The processor of claim 13 wherein said value is to be incremented geometrically by left-shifting a binary 1 bit into said value.

15. (Currently Amended) A processor to handle processing of at least first and second threads in parallel, comprising:

control logic to assign priority to said first thread and to assign priority to said second thread in response to one of a plurality of conditions being true, the conditions ~~including~~consisiting

if a processing counter expires;

if processing of said first thread retires an instruction from said first thread; and

if there is not an indication of approaching instruction side starvation for said first thread.

16. (Currently Amended) The processor of claim 15 wherein said indication of approaching instruction side starvation for said first thread includes each of a plurality of conditions being true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

17. (Original) A computer system to handle processing of at least first and second threads in parallel, comprising:

a memory to store instructions for first and second threads;

a processor including

control logic coupled to said memory to assign priority between said first and second threads;

a thread precedence counter coupled to said control logic wherein priority is assigned to said second thread after said thread precedence counter expires.

18. (Original) The computer system of claim 17 wherein a preliminary value for said thread precedence counter is based on a value stored in a first starting counter associated with said first thread.

19. (Currently Amended) The computer system of claim 18 wherein said control logic is to determine if there is an indication of approaching instruction side starvation for said first thread and to increment a value stored in said first starting counter ~~is incremented~~ in response to an indication of approaching instruction side starvation for said first thread.

20. (Currently Amended) The computer system of claim 19 wherein said control logic is determine if there is an indication of approaching instruction side starvation for said first thread by determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

21. (Original) The computer system of claim 20 wherein said control logic is to increment the value stored in the first starting counter geometrically.

22. (Original) The computer system of claim 21 wherein said value is to be incremented geometrically by left-shifting a binary 1 bit into said value.

23. (Currently Amended) A computer system to handle processing of at least first and second threads in parallel, comprising:

a memory to store instructions for first and second threads;

a processor including

control logic to assign priority to said first thread and to assign priority to said second thread in response to one of a plurality of conditions being true, the conditions ~~including~~consisting:

if a thread precedence counter expires;

if processing of said first thread retires an instruction from said first thread; and

if there is not an indication of approaching instruction side starvation for said first thread.

24. (Currently Amended) The computer system of claim 23 wherein said indication of approaching instruction side starvation for said first thread includes each of a plurality of conditions being true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

25. (Original) A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor to handle processing of at least first and second threads in parallel and assign thread priority comprising:

assigning priority to said first thread;

loading a preliminary value to a thread precedence counter; and

assigning priority to said second thread after said thread precedence counter expires.

26. (Original) The set of instructions of claim 25 wherein said preliminary value is based on a value stored in a first starting counter associated with said first thread.

27. (Currently Amended) The set of instructions of claim 26 wherein the ~~method~~set of instructions further includes

determining if there is an indication of approaching instruction side starvation for said first thread; and

incrementing a value stored in said first starting counter is incremented in response to an indication of approaching instruction side starvation for said first thread.

28. (Currently Amended) The set of instructions of claim 27 wherein determining if there is an indication of approaching instruction side starvation for said first thread includes determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

29. (Original) The set of instructions of claim 28 wherein when incrementing the value stored in the first starting counter, said value is incremented geometrically.

30. (Original) The set of instructions of claim 29 wherein said value is incremented geometrically by left-shifting a binary 1 bit into said value.